Appl. No. 10/718,608 Response filed December 9, 2004 Reply to Office Action of September 9, 2004

Amendments to the Abstract

The Abstract is amended as follows: [Problems] To provide an oscillation circuit which feeds clocks of low skew and low jitter to the logic circuit and memory-circuit of a microprocessor or the like, and also to provide a semiconductor integrated circuit device of high speed by the use of the oscillation circuit. [Means for Resolution] In an The oscillation circuit includesing the principal means of the present invention, at least two ring oscillation circuits in each of which a plurality of inverters are connected in a ring shape in a multi-stage fashion, and a conductive wiring line+. Tthe output of at least one inverter of each of the ring oscillation circuits is connected to the conductive wiring line, whereby the plurality of ring oscillators are caused to oscillate at an identical frequency. A PLL is constructed in such a way that the oscillation circuit obtained by the above means is formed into a voltage-controlled oscillation circuit, and that a phase-frequency comparator, a charge pump circuit and a low-pass filter are employed. Besides, clocks are distributed within a semiconductor circuit device in such a way that the conductive wiring line of the oscillation circuit Appl. No. 10/718,608 Response filed December 9, 2004 Reply to Office Action of September 9, 2004

of the PLL is used for a-global clock, and that clock distribution systems are connected.

[Effects] It is permitted to feed clocks of low skew and low jitter to the logic circuit and memory-circuit of a microprocessor or the like, and a semiconductor integrated circuit device of high speed can also be realized owing to the feed of the clocks.